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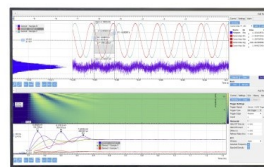
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# MODEL-BASED SILICON WAFER CRITERIA FOR OPTIMAL INTEGRATED CIRCUIT PERFORMANCE

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The Starting Materials requirements in the 1997 Semiconductor Industry Association (SIA) National Technology Roadmap for Semiconductors (NTRS) were developed by a fifty-nine member team comprised of industrial (e.g., silicon suppliers, equipment and IC manufacturers) and university personnel. The silicon wafer parameter values as-received by the IC manufacturers are generally derived from model-based analyses based on the technology generation critical dimension (CD), bits, wafer diameter, etc. The values represent the perceived critical material characteristics required to ensure that silicon materials support the continued growth of the IC industry while being cognizant of cost-of-ownership (CoO) considerations. The characteristics were developed via a modular approach of a core set of general characteristics applicable to all product wafers, plus specific recommendations for polished, epitaxial and silicon-on-insulator (SOI) wafers. The formulae utilized, assumptions made and the issues involved, as well as opportunities for improvements in the modeling process, are discussed.

## INTRODUCTION

The fabrication of a state-of-the-art DRAM, microprocessor or application specific integrated circuit (ASIC) has become a truly complex manufacturing process with over 500 significant process steps. A paradigm shift has concurrently occurred during the '90's with an increased emphasis towards the scientific understanding of the physico-chemical processes and the selective application of design-of-experiment methodologies in the improved fabrication of ICs. Indeed, model-based experiments and simulation procedures have become *de rigeur* in the IC industry with technology advancements based on scientific principles rather than exclusively experience per se. This approach has especially focused on front-end-of-the-line (FEOL) core processes associated with transistor formation (e.g., dielectric, electrode and plasma etching) in conjunction with component isolation, shallow p-n junction formation and contact structures with the impending sub-100 nm era. The FEOL section of the NTRS includes Starting

Materials, Surface Preparation, Thermal/Thin Film and Doping, and related plasma etching phenomena (1). Although the Starting Materials requirements must be supportive in achieving these device structures, it is especially important to balance the "best wafer possible" against the cost-of-ownership (CoO) opportunity of not driving silicon requirements to the detection or ultimate resolution limit but to some less stringent and optimized value (2,3). For example, the incoming Starting Material wafer contamination values are greater than the analogous requirements for pre-gate Surface Preparation cleans due to CoO considerations (1).

The Starting Material wafer parameter values as-received by the IC manufacturers are generally derived from model-based analyses based on the technology generation critical dimension (CD), bits, wafer diameter, etc. The understanding of these underlying models of IC performance-characteristic relationships is, in fact, more critical than the specific numerical values. Although empirical models are employed utilizing extrapolated

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trends, as appropriate, the use of anecdotal opinions was minimized. A fifty-nine member team comprised of industrial (e.g., silicon suppliers, equipment and IC manufacturers) and university personnel was formed to identify the required metrics, including the formulae, assumptions and issues involved (see Table 1). The Starting Materials characteristics were developed via a modular approach of a core set of general characteristics

applicable to all product wafers as-received by the IC manufacturers plus specific recommendations for polished, epitaxial and silicon-on-insulator (SOI) wafers. The Starting Materials values represent the perceived critical material characteristics required to ensure that silicon materials support the continued productivity growth of the IC industry as described by Moore's law (4-7).

Table 1  
Starting Materials Sub-Teams and Personnel for NTRS

Model-based Structured Approach	Statistical Distributions/ Metrology	Polished Wafer Trends	Epitaxy Wafer Trends	SOI	Corresponding Consultants
Randy Goodall	Larry Beckwith	Steve Bay	Chi Au	Mike Alles	Olli Anttila
Kim Kimerling	<b>Murray Bullis</b>	Jeff Butterbaugh	Michael Brohl	George Cellar	Werner Bergholz
Harold Korb	Alain Diebold	John Crabtree	Jeff Epstein	Harry Hovel	Cor Claeys
David Jensen	Worth Henley	Bob Graupner	Dinesh Gupta	Pat O'Hagan	Laszlo Fabry
Lubek Jastrzebski	Paul Langer	Dick Hockett	Bob Helms	George Rozgonyi	Dieter Huber*
Harold (Skip) G. Parks	Larry Larson	Bob Johnston	<b>Fritz Kirscht</b>	Witek Maszara	Bill Lynch
K.V. Ravi	Don McCormack	Bob Kunesh	Wen Lin	Dieter Schroder	Mike Mendicino
Eicke Weber	Richard Novak	<b>Jim Moreland</b>	Fred Meyer	Paul Smith	J-G Park
	Chris Sparks	Jagdish Prasad	David Myers	<b>Syd Wilson</b>	Paul Patruno
		Larry Shive	P.K. Vasudev		Jon Rossi
		Mike Walden			Shin Takasu
					Masaharu Watanabe

\* Deceased

## WAFER AREA GENERATION MODEL

The phenomenal growth of the IC industry, evidenced by a 25-30% compound annual growth rate (CAGR)—achieved by staying on the “productivity learning curve”—continues to be the gauge by which the industry is measured (6,7). Concurrently, the number of transistors per chip has increased with a CAGR of approximately 40% such that the number of transistors is over 10 million on a state-of-the-art microprocessor (1). This enables a 25-30% per year cost reduction per function for nearly the past thirty years. This growth has been fueled by four factors, (a) shrinking lithographic

design rules; (b) yield improvements; (c) increased equipment utilization and (d) larger wafer diameter (8). The largest opportunity growth factor to maintain the IC productivity engine is increased equipment effectiveness; that is, the percentage of time the equipment is adding value to the wafer (8). This is especially important inasmuch as the largest challenge to maintaining the productivity curve may be the enormous financial infrastructure required, rather than technological limits, to increase chip density (6,9,10). Indeed, departures from Moore's law have already been noted (6). Nevertheless, increased wafer diameter has been an historical method by which the number of IC chips per wafer has been

increased. The conversion to 300 mm diameter wafers, beginning about 1998-1999, with initiation of volume manufacturing expected about 2000-2001, is necessary to maintain the required economy of scale for large volume IC manufacturing. Business issues are the primary migration concern as it appears the engineering issues associated with the cost-effective crystal growth (11) and wafer gravitational stresses (10) can be addressed. It should be noted, however, that new design rule super-shrinks, resulting in increased numbers of chips per wafer, might delay the onset of volume conversion by a year from earlier projections. Figure 1 illustrates the historical area demand for silicon per year versus year for wafer diameter from 38/51 mm to the present era and the prognosis for future diameters (12). As a given diameter nears the peak of its utilization, initiation of the next diameter must begin. Projections of the wafer diameter beyond 300 mm suggest that 450 mm (followed by 675 mm) may be the appropriate next sizes to maintain the

historical productivity enhancement growth rate (12), modeled by a doubling of the wafer area for the next generation wafer size. These future wafer diameters, however, will require the most severe business and economic global discussions before their projected implementation becomes a reality (see the Summary section).

Concurrently, the edge exclusion is projected to decrease from 3 to 1 mm (see Table 2). The decreasing edge exclusion has a second order effect on increasing the number of chips per wafer due to the more effective layout of rectangular chips on a larger diameter (e.g. circular) wafer. Indeed, in some cases, wafer specifications are denoted over the whole wafer albeit there may be temporary limitations in productivity increase due to metrology issues and the fact that nearly all IC processes have significant edge exclusions.

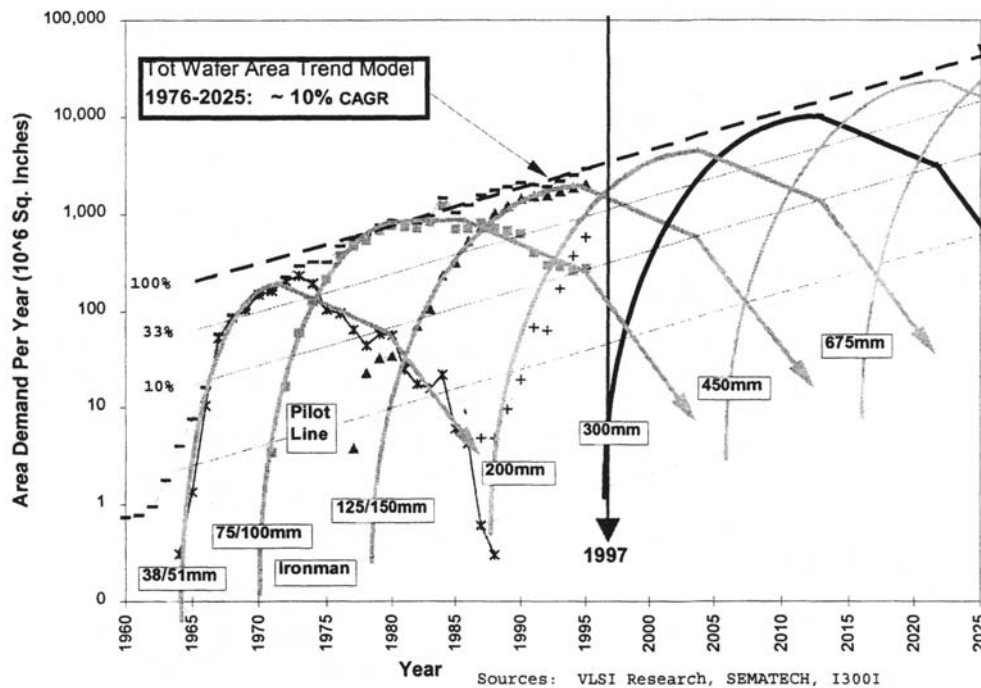


Figure 1 - Modeled Wafer Area Demand Per Year (updated from [12] ).

Table 2  
Wafer Diameter and Edge Exclusion With Technology Generation

Year of First Product Shipment Technology Generation	1997 250 nm	1999 180 nm	2001 150 nm	2003 130 nm	2006 100 nm	2009 70 nm	2012 50 nm
Wafer Diameter (mm)	200	300	300	300	300	450	450
Edge Exclusion (mm)	3	2	2	2	1	1	1
	Solutions Exist	Solutions Being Pursued			No Known Solution		

## YIELD-DEFECT DENSITY MODEL

The lack of effective, experimentally based data or models at the present time precludes mutually constraining several parameters by partitioning their yield impact (i.e., assuming they are statistically dependent) and, therefore, the parameters are taken as statistically independent. The numerical values of the parameters are selected as upper limits corresponding to 99% yield for each characteristic parameter. It is assumed that the median value of the typically manufactured distribution for each parameter is much better (e.g. usually smaller) than the listed value and that the upper limit values would rarely coincide for more than one parameter at a time on a silicon wafer, thereby ensuring the total yield for all parameters is about 99% (1). This approach is expected to provide the most cost-effective solution to wafer quality since it is essential to balance the “best wafer possible” against the CoO opportunity of not driving silicon requirements to the detection or ultimate resolution limit but to some less stringent and optimal value(2,3).

The Poisson probability distribution (13) is generally expressed:

$$Y = \exp [-D_e A_{\text{active}}] \quad (1)$$

where  $D_e$  is the electrical defect density per  $\text{cm}^2$  and  $A_{\text{active}}$  is the active chip area ( $\text{cm}^2$ ). More significantly,  $D_e$  is related to the physical defect density per  $\text{cm}^2$  through the kill ratio,  $R_i$ , for defect type  $i$  and  $A_{\text{active}}$  is replaced by the total chip area,  $A_{\text{chip}}$ , through the critical area ratio,  $\alpha$ , expressed, respectively, by:

$$D_e = \sum_i R_i D_i \quad (2a)$$

$$A_{\text{active}} = \alpha A_{\text{chip}} \quad (2b)$$

Equation (1) may, therefore, be replaced by:

$$Y = \exp \left[ -\sum_i D_i R_i (\alpha A_{\text{chip}}) \right] \quad (3)$$

The critical area ratio,  $\alpha$ , is expressed as the total number of transistors per chip,  $T$ , for an MPU or the number of bits per chip for a DRAM, divided by the chip area, multiplied by three terms which take into account the area per transistor or active device component as expressed by eq. 4. These terms are, (a) the square of the CD of the basic “unit cell” making up the device component;  $\beta$ , the width to length ratio of the unit cell; and,  $\delta$ , the number of unit cells required to fabricate the device component of interest.

$$\alpha = (T/A_{\text{chip}}) (CD)^2 \beta \delta \quad (4)$$

For a DRAM,  $\beta_{\text{DRAM}} = 1$  whereas for logic ICs,  $\beta_{\text{LOGIC}}$  is modeled as 10, although values of  $\beta_{\text{LOGIC}}$  can range from approximately five to 20. Delta,  $\delta$ , varies from unity for a gate oxide integrity (GOI) test to six for a buried oxide,  $\text{BOX}$ , structure in the case of SOI. Replacing eq. 4 in eq. 3, one obtains the basic, modified Poisson probability distribution relating the yield to the defect density:

$$Y = \exp \left[ -\sum_i D_i R_i \{T (CD)^2 \beta \delta\} \right] \quad (5)$$

A major assumption in the current model, clearly requiring rectification, is the representation of  $D_i$  as a fixed defect size with fixed kill ratio,  $R_i$ , for all defect sizes, rather than determining an effective value by integration over the particle size and kill ratio distribution. Table 3 summarizes the relevant CDs, transistors per chip, bits per chip and the MPU and DRAM chip area, critical area and critical area ratios.

Table 3  
Critical Dimension, Transistors Per Chip, Bits Per Chip, MPU and DRAM Areas, Critical Areas and Critical Area Ratios  
With Technology Generation

### Microprocessor

Year	CD (cm)	Transistors / Chip	MPU Area (cm <sup>2</sup> )	MPU Critical Area (cm <sup>2</sup> )	MPU Critical Area Ratio
1997	2.50x10 <sup>-5</sup>	1.1x10 <sup>+7</sup>	3.0	6.88x10 <sup>-2</sup>	2.29x10 <sup>-2</sup>
1999	1.8x10 <sup>-5</sup>	2.1x10 <sup>+7</sup>	3.4	6.80x10 <sup>-2</sup>	2.00x10 <sup>-2</sup>
2001	1.5x10 <sup>-5</sup>	4.0x10 <sup>+7</sup>	3.85	9.0x10 <sup>-2</sup>	2.34x10 <sup>-2</sup>
2003	1.3x10 <sup>-5</sup>	7.6x10 <sup>+7</sup>	4.3	1.28x10 <sup>-1</sup>	2.98x10 <sup>-2</sup>
2006	1.0x10 <sup>-5</sup>	2.0x10 <sup>+8</sup>	5.2	2.00x10 <sup>-1</sup>	3.85x10 <sup>-2</sup>
2009	7.0x10 <sup>-6</sup>	5.2x10 <sup>+8</sup>	6.2	2.55x10 <sup>-1</sup>	4.11x10 <sup>-2</sup>
2012	5.0x10 <sup>-6</sup>	1.4x10 <sup>+9</sup>	7.5	3.5x10 <sup>-1</sup>	4.67x10 <sup>-2</sup>

### DRAM

Year	CD (cm)	Bits / Chip	DRAM Area (cm <sup>2</sup> )	DRAM Critical Area (cm <sup>2</sup> )	DRAM Critical Area Ratio
1997	2.50x10 <sup>-5</sup>	2.67x10 <sup>+8</sup>	2.8	0.167	5.96x10 <sup>-2</sup>
1999	1.8x10 <sup>-5</sup>	1.07x10 <sup>+9</sup>	4.0	0.347	8.68x10 <sup>-2</sup>
2001	1.5x10 <sup>-5</sup>	1.7x10 <sup>+9</sup>	4.5	0.383	8.61x10 <sup>-2</sup>
2003	1.3x10 <sup>-5</sup>	4.29x10 <sup>+9</sup>	5.6	0.725	1.29x10 <sup>-1</sup>
2006	1.0x10 <sup>-5</sup>	1.72x10 <sup>+10</sup>	7.9	1.72	2.18x10 <sup>-1</sup>
2009	7.0x10 <sup>-6</sup>	6.87x10 <sup>+10</sup>	11.2	3.36	3.0x10 <sup>-1</sup>
2012	5.0x10 <sup>-6</sup>	2.75x10 <sup>+11</sup>	15.8	6.88	4.35x10 <sup>-1</sup>

## STARTING MATERIALS PARAMETERS

The starting materials parameters discussed below are highlighted in terms of the formulae, assumptions and issues requiring further clarification. The various physical phenomena, however, are not discussed per se, but referenced to the current literature as appropriate for more detailed discussions.

### Localized Light Scatterer (LLS)

The localized light scatterer, *LLS*, size is modeled as:

$$\text{Size} = K_1 \times (\text{CD}) \text{ (nm)} \quad (6)$$

with  $K_1 = 0.5$  and CD in nm. The LLS defect density (which includes particles; crystal originated pits, COPs; residual polishing micro-damage; surface microroughness; surface chemical residues including organics; and structural defects such as epitaxial stacking faults) (14) is modeled by the modified Poisson

probability distribution of Eq. 5 with the yield  $Y_{LLS} = 99\%$ , LLS kill ratio  $R_{LLS} = 0.1$ ,  $\beta = 1$  and  $\delta = 1$  (see Table 4). The particle density is empirically modeled (15) as:

$$\text{Particle Density} = K_2 \times (\text{CD})^{1.42} \text{ (cm}^{-2}\text{)} \quad (7)$$

with  $K_2 = 5.50 \times 10^{-5}$  and CD is in nm. A major assumption in this empirical model is the extrapolation of the particle density from the regime where COPs is insignificant (15) to the less than 150 nm technology generation, where COPs become significant for polished wafers. The value of  $R_{LLS}$  for Starting Materials,  $R_{LLS} = 0.1$ , is one-half the value utilized for Surface Preparation with its emphasis on pre-gate cleans, due to CoO considerations (see Table 4). That is, the wafer supplier performs a final clean while the IC manufacturer often performs an incoming clean as well as a number of cleans prior to gate oxidation; accordingly, the incoming surface particles and metals requirements are less stringent than the pre-gate oxidation requirements. Nevertheless, a more rigorous determination of the kill ratio,  $R_{LLS}$ , its

functional dependence on size, and the development of compatible metrology tools must also be addressed.

Both the chemical structure of the wafer surface produced and delivered by the wafer supplier (hydrophobic versus hydrophilic) and the wafer-shipping box interaction are critical issues in controlling the subsequent adsorption of metals, ionics, organics and particles on the wafer surface. The physical structure of the silicon surface has also

emerged as a critical concern. Both polished and epitaxial surfaces exhibit defects that must be controlled to achieve high yielding ICs. The detection, counting, compositional analysis, morphology, removal and prevention of surface defects are state-of-the-art challenges for both metrology and silicon wafer technology as is the development of laser scanning and other instrumentation utilized to monitor these defects.

Table 4  
LLS and Particle Densities for Starting Materials and Surface Preparation With Technology Generation

Year of First Product Shipment Technology Generation	1997 250 nm	1999 180 nm	2001 150 nm	2003 130 nm	2006 100 nm	2009 70 nm	2012 50 nm
<b>LOCALIZED LIGHT SCATTERERS (LLS) SIZE</b> (includes particles) (nm)	125	90	75	65	50	35	25
<b>LLS: STARTING MATERIALS</b> Total (cm <sup>-2</sup> )	≤ 0.60	≤ 0.29	≤ 0.26	≤ 0.14	≤ 0.06	≤ 0.03	≤ 0.015
Particles (#/cm <sup>2</sup> )	≤ 0.14	≤ 0.088	≤ 0.068	≤ 0.055	≤ 0.038	≤ 0.023	≤ 0.014
<b>LLS: SURFACE PREPARATION</b> Total (cm <sup>-2</sup> )	≤ 0.30	≤ 0.15	≤ 0.13	≤ 0.07	≤ 0.03	≤ 0.015	≤ 0.007

Additionally, the wafer back-surface is increasingly being prepared with a shiny or polished finish to improve flatness, the uniformity of monitoring the wafer temperature during IC processes and, where applicable, distinguishing particles and crystal micro-defects such as COPs from microroughness for ULSI cleanliness requirements. The improvement in back-surface cleanliness, however, more readily reveals microscopic contamination and handling scratch damage from robotic handling systems. Standards for robotic handlers may be necessary to ensure conformance of the surface to the implicit quality requirements.

#### Organics/Polymers and Surface Microroughness

Organics and polymers are assumed to be sufficiently innocuous if modeled as approximately 0.1 of a monolayer (e.g.  $\leq 1 \times 10^{14}/\text{cm}^2$ ). Oxygen-free ambients can vaporize organics (16). Other studies indicate that increased numbers of residual surface carbon atoms can reduce the charge-to-breakdown ( $Q_{bd}$ ) for gate oxide integrity (GOI) tests (17). Nevertheless, it is expected that the wafer container will tend to saturate the surface with organics and it may be appropriate to only specify organics for the Surface Preparation roadmap. Clearly, this is an area requiring further clarification (18).

The front-surface microroughness has been taken as  $\leq 0.10$  nm for all technology generations except  $\leq 0.15$  nm at the 250 nm technology node. The instrumentation choice, target values and spatial

frequency range (scan size) selected should be based on the application (19). The power spectral density analysis is recommended to fully utilize the currently accessible spatial frequency range of  $0.01\text{-}50 \mu\text{m}^{-1}$  using atomic force microscopy (AFM). The effects of different surface termination and the wafer-carrier as well as storage ambient on surface microroughness are critical issues that are not yet sufficiently comprehended for optimal device/IC performance.

#### Surface Metals - Critical Metals

The critical surface metals are modeled by the modified Poisson probability distribution Eq. 5 with the yield  $Y_M = 99\%$ , metal kill ratio  $R_M = 1$ ,  $\beta = 1$  and  $\delta = 1$ . The metal kill ratio  $R_M$  is taken as unity, which implies that every metal is an equally effective generation-recombination (g-r) defect center. This, of course, is inappropriate inasmuch as the effectiveness of a g-r center depends on its energy level relative to mid-gap, its capture cross-section, etc. Furthermore, metallics are most detrimental when they decorate structural irregularities in space-charge regions (20,21) rather than as g-r centers per se. Nevertheless, we have utilized this zeroeth order approximation, in conjunction with an empirically derived relation between the metal (Fe) defect density ( $D_M$ ) and critical metal (Fe) surface concentration [M] noted by Eq. 8, from which [M] is determined in conjunction with Eq. 5:

$$D_M = K_3 [M]^3 \exp(-T_o/0.7 \text{ nm}) (\text{cm}^2) \quad (8)$$

with  $K_3 = 1.854 \times 10^{-29} \text{ cm}^4$  and  $T_o$  is the equivalent oxide thickness in nm for each technology generation. The experimental data in this model (see Table 5) are based on experimentation which extends the precursor publication of oxide films to the 8 nm regime (22,23). Nevertheless, eq. 8 is not based on experiments in the sub 4 nm regime and, therefore, the mechanism and dependence of the oxide breakdown with surface metallics, such as Fe, may not be adequately represented by extrapolation of the experimental data. The experimental data for Fe, furthermore, has been extended to include critical metals such as Ca, Co, Cu, Cr, K, Mo, Mn, Na and Ni, although all these metals redistribute differently between the

silicon surface and the growing oxide (22-24). The model analysis explicitly assumes that the listed value corresponds to the highest of the several possible candidate metals, with the other metals more likely near the mean of their distribution and, thereby, exhibiting a yield much greater than 99%. Clearly, it appears that herein is an opportunity for a partitioning scheme. The Starting Materials critical metals are approximately 4x the Surface Preparation pre-gate values, consistent with the CoO approach. If the IC manufacturer uses an initial cleaning process, one may group K and Na with the other surface metals (see below). The present analysis assumes the presence of a wafer gettering mechanism which, if not present, would decrease the Starting Materials critical metal concentration by a factor of 2x.

Table 5  
Critical Surface Metal Densities for Starting Materials and Surface Preparation With Technology Generation

Year of First Product Shipment Technology Generation	1997 250 nm	1999 180 nm	2001 150 nm	2003 130 nm	2006 100 nm	2009 70 nm	2012 50 nm
CRITICAL SURFACE METALS Starting Materials (at/cm <sup>2</sup> )	$\leq 2.5 \times 10^{10}$	$\leq 1.3 \times 10^{10}$	$\leq 1 \times 10^{10}$	$\leq 7.5 \times 10^9$	$\leq 5 \times 10^9$	$\leq 2.5 \times 10^9$	$\leq 2.5 \times 10^9$
CRITICAL SURFACE METALS Surface Preparation (at/cm <sup>2</sup> )	$\leq 5 \times 10^9$	$\leq 4 \times 10^9$	$\leq 3 \times 10^9$	$\leq 2 \times 10^9$	$\leq 1 \times 10^9$	$\leq 10^9$	$\leq 10^9$

### Surface Metals - Other Metals

Other surface metals include Al, Ti, V and Zn, which were assigned a value of  $10^{11}/\text{cm}^2$  for all technology generations; here also, the presence of a wafer gettering mechanism is assumed. The Al value is the maximum surface concentration to prevent modification of silicon's oxidation rate (25); Al also forms charged defects in the oxide which may require consideration (26).

### Site Flatness

The site front-surface least squares reference plane total indicator range flatness (SFQR) (27) is modeled by equating it to the critical dimension (CD) for dense lines (DRAM half pitch) for each technology generation, including partial sites, by:

$$\text{SFQR} = K_4 \times (\text{CD}) \quad (9)$$

with  $K_4 = 1$ . For isolated lines (MPU Gates), the CD is approximately 80% of the dense line values for technology generations  $\geq 130$  nm and approximately 70% for technology generations  $< 130$  nm (see Table 6), although this does not

impact the SFQR requirements. Recent epitaxial wafer SFQR values for a number of suppliers are consistent with 250 nm and 180 nm DRAM requirements and correspond to approximately 25% and 20% of the allowable depth-of-focus for the 250 nm and 180 nm technology generations, respectively (see Table 6) (28). Double-side polishing utilized on 300 mm wafers (as well as for 200 mm wafers) is expected to result in significantly improved site flatness. Scanning steppers are expected to be implemented, in some cases, for technology generations  $\leq 180$  nm and utilization of the new site flatness metric, SFSR (29,30) (site front-surface scanning total indicator range) will be required. Non-optical lithography may be required for technology generations  $\leq 100$  nm in which case the site flatness may be de-coupled from the CD. Finally, warp is selected to be less than 50  $\mu\text{m}$  for all CD generations, taking into consideration different back-surface films. However, significantly improved bow and warp performance for both 200 mm and 300 mm diameter wafers is expected in the case of wire-sawing and the relevance of these parameters is expected to decrease (28,31).

Table 6  
Several Site Flatness and Related Parameters With Technology Generation

Year of First Product Shipment Technology Generation	1997 250 nm	1999 180 nm	2001 150 nm	2003 130 nm	2006 100 nm	2009 70 nm	2012 50 nm
Dense Lines (DRAM Half Pitch) *	250	180	150	130	100	70	50
Isolated lines (MPU Gates) *	200	140	120	100	70	50	35
Site Flatness (SFQR) (nm)	≤ 250	≤ 180	≤ 150	≤ 130	≤ 100	≤ 100	≤ 100
Site Size (mm x mm)	22 x 22	25 x 32	25 x 34	25 x 36	25 x 40	25 x 44	25 x 52
Site Area (mm <sup>2</sup> )	484	800	850	900	1000	1100 **	1300 **
Depth of focus (μm, usable @ full field with ± 10% exposure)	0.8	0.7	0.6	0.6	0.5	0.5	0.5

\* Requirements scale with resolution for shrinks

\*\* Site size requirements are based on Year 2 chip sizes, the year demanding the full site size for high volume production

### Oxygen

The values for oxygen and bulk micro-defects (BMD) are based on extensive anecdotal evidence. The oxygen values represent the range of the center point requirement to provide internal gettering (IG) for generally high oxygen values or minimal IG for lower oxygen values, based on experimentally derived IC requirements. The tolerance of ± 1.5 parts per million atomic (ppma) represents the min-max range about the center point value; a tolerance of ± 2 ppma is appropriate for the 250 nm technology generation (see Table 7). Bulk micro-defects (BMD) in IG (no IG) polished wafers are  $> 1 \times 10^8/\text{cm}^3$  ( $< 1 \times 10^7/\text{cm}^3$ ) after IC processing. The oxygen, BMD value and the relationship between them providing effective IG requires a more rigorous examination

inasmuch as the formation of uncontrolled BMD (e.g.,  $\text{SiO}_x$  precipitates) in both polished and epitaxial wafers, may result in excessive device leakage current, necessitating the optimization of IG (32). The magnitude and uniformity requirements for oxygen, as well as dopants, may require the utilization of magnetic Czochralski (MCZ) silicon, especially for 300 mm and larger diameter wafers (33).

The determination of the BMD density ( $\text{cm}^{-3}$ ) by preferential etching requires accurately monitoring the silicon etch rate in order to convert the area density to a volume density. The measurement of interstitial oxygen and the accompanying acceleration of BMD formation in heavily doped silicon continues to remain an area of active research (34).

Table 7  
Oxygen Concentration and Tolerance With Technology Generation

Year of First Product Shipment Technology Generation	1997 250 nm	1999 180 nm	2001 150 nm	2003 130 nm	2006 100 nm	2009 70 nm	2012 50 nm
Oxygen (Tolerance ± 1.5 ppma) (ASTM '79)	20 - 31	19 - 31	18 - 31	18 - 31	18 - 31	18 - 31	18 - 31

Recently, the characterization of the time dependence of oxygen precipitation has been studied in 300 mm sectioned polished wafers using the Avrami relation (28,31,35) as described by:

$$\xi = 1 - \exp [-kt^n] \quad (10)$$

where  $\xi$  is the fraction transformed (e.g., precipitated) material and  $n$  and  $k$  are parameters characteristic of the precipitation kinetics. The  $n$  parameter relates to the dimension (3D, 2D, fractal) of the system participating in the polymorphic change and is also influenced by the growth mechanism of an individual island (28,31). The  $k$  parameter is proportional to the number of nucleation sites and is governed by the mechanism of individual

island growth at the phase boundary, e.g., diffusion-limited, reaction-limited, capture at the perimeter, etc. (36). A detailed discussion of the Avrami analysis and the kinetic parameters  $n$  and  $k$  (determined by the slope and intercept, respectively), with  $O_i^\circ$  have been presented (28,31). The results appear consistent with the present understanding of oxygen in silicon (37,38) and may be useful to enhance our understanding of the precipitation kinetics of oxygen in silicon. It has been noted, however, that  $n$  and  $k$  cannot uniquely determine the rate limiting processes inasmuch as the different mechanisms noted above sometimes yield similar values for  $n$  and  $k$  (28). These topics continue to remain at the forefront of silicon technology (39).

The above analysis does not explicitly address the coupling of the thermal history of the crystal, the variation of  $O_i^\circ$  along the crystal axis and the BMD formation during subsequent wafer thermal processes and IC fabrication. The decoupling of the oxygen content and the IC process details from the BMD density and the denuded zone (DZ) depth, using vacancy concentration engineering techniques, may be required (40-42). The utilization of an appropriate thermal anneal requires a fundamental understanding of the critical temperature range for vacancy agglomeration (COPs, D-defects) and oxygen precipitation control (40-45). For example, the dependence of  $\Delta O_i$  versus  $O_i^\circ$  has been shown to exhibit a rather weak dependence with  $O_i^\circ$ , compared to the previous cases (41,46). This technique offers the opportunity to tune the BMD depending only upon the  $O_i^\circ$  value inasmuch as the thermal history has been decoupled from the BMD formation (41). Quantitative formulation of this methodology will facilitate model-based BMD formation by tuning the crystal growth parameters to minimize the formation of undesired point-defect clusters. The IC DRAM process flow, however, may also need to be re-engineered, in partnership with the silicon supplier, to ensure mutual compatibility.

### Carrier Lifetime

The carrier diffusion length,  $L$ , is related to the bulk carrier recombination lifetime,  $\tau_r$ , by:

$$L = \sqrt{D_n \tau_r} \quad (11)$$

where  $D_n$  is the minority-carrier diffusion coefficient (47-49). The latter is taken as representative of lightly doped

p-type material at 27°C (34.5 cm<sup>2</sup>/s). The carrier diffusion length is modeled as equal to the wafer thickness by:

$$L \equiv \text{wafer thickness} \quad (12)$$

and is therefore dependent on the technology generation since the wafer thickness increases as the wafer diameter increases. Equation (11) is accordingly written as:

$$\tau_r = 2 (\text{wafer thickness})^2 / D_n \quad (13)$$

where the factor two enters in because  $\tau_r$  has been implicitly partitioned evenly between the silicon supplier and the IC manufacturer. Appropriate techniques to control, passivate or correct for surface effects are mandatory when measuring  $\tau_r$ . The bulk carrier recombination lifetime is a measure of the cumulative effect of all the metals. Iron, however, is a common contaminant and the bulk carrier recombination lifetime listed for the 250 nm technology generation in Table 8 is consistent with recent state-of-the-art experimental Fe concentrations (50). Iron concentrations  $\leq 1 \times 10^{10}$  /cm<sup>3</sup>, however, may not impact a proportionally significant carrier lifetime improvement because of the influence of residual crystalline flaws in the silicon material (51,52), although one might expect larger values for  $\tau_r$  even for today's technology. Relating the carrier diffusion length to the wafer thickness as is presently the case, however, is rather artificial and precludes accountability to the material physics issues; clearly, rectification of this model analysis is required. In any case, it should be noted that the bulk Fe concentration (cm<sup>-3</sup>) cannot be converted to its surface value (cm<sup>-2</sup>) via the wafer thickness due to thermodynamic distribution effects (2,24).

The SOI effective recombination lifetime,  $\tau_{r,eff}$ , is represented by:

$$(\tau_{r,eff})^{-1} = (\text{SOI layer thickness}/2s)^{-1} + (\tau_{r,bulk})^{-1} \quad (14)$$

where  $s$ , the surface recombination velocity, is taken as 1-10 cm/s in this model calculation. Here also, proper control, passivation or correction for surface effects at the upper silicon surface is required. Future model improvements should properly account for the surface recombination velocity at the silicon/BOX interface. Since  $\tau_{r,bulk}$  is several orders of magnitude larger than the reciprocal of the first term in Eq. (14), the value for  $\tau_{r,eff}$  is approximately represented as  $(2s/\text{SOI layer thickness})$  (see Table 8).

Table 8  
Bulk Carrier Recombination Lifetime, Bulk Fe Concentration and Effective SOI Recombination Lifetime With Technology Generation

Year of First Product Shipment Technology Generation	1997 250 nm	1999 180 nm	2001 150 nm	2003 130 nm	2006 100 nm	2009 70 nm	2012 50 nm
Recombination Lifetime ( $\mu$ s)	$\geq 300$	$\geq 325$	$\geq 325$	$\geq 325$	$\geq 325$	$\geq 450$	$\geq 450$
Total bulk Fe (at/cm <sup>3</sup> )	$3 \times 10^{10}$	$1 \times 10^{10}$	$1 \times 10^{10}$	$< 1 \times 10^{10}$	$< 1 \times 10^{10}$	$< 1 \times 10^{10}$	$< 1 \times 10^{10}$
Effective SOI Recombination Lifetime ( $\mu$ s)	0.3	0.4	0.5	0.6	1	1	1

The generation lifetime,  $\tau_g$ , is a harbinger of device performance in, for example, a DRAM refresh operation. This lifetime parameter has been modeled by considering only space-charge region leakage currents. We have neglected contributions due to the device sub-threshold, gate dielectric, and diffusion leakage currents, which represents a shortcoming of the current model for the first two components. Accordingly,  $\tau_g$  is modeled utilizing the definition of  $\tau_g$  by Eq. 15 (47), where the generation rate,  $g$ , is considered to represent only space-charge region leakage:

$$\tau_g = n_i/g \quad (15)$$

Accordingly,  $\tau_g$  is represented by:

$$\tau_g = (qWn_i) (I_{limit} / A_{space-charge})^{-1} \quad (16)$$

where  $q$  is the absolute value of the electron charge ( $1.602 \times 10^{-19}$  coulomb),  $W$  is the space-charge region width (taken as  $0.5 \mu\text{m}$ ) and  $n_i$  is approximately  $1.02 \times 10^{10}/\text{cm}^3$  at  $27^\circ\text{C}$  and  $1.4 \times 10^{12}/\text{cm}^3$  at  $100^\circ\text{C}$  (53,54). The value of  $(I_{limit}/A_{space-charge})$  is modeled by taking the leakage current,  $I_{limit}$ ,  $\leq 10^{-16}$  A/bit at  $27^\circ\text{C}$  ( $\leq 10^{-13}$  A/bit at  $100^\circ\text{C}$ ) (55-58) and the total space-charge area of a trench storage cell for the 256 MDRAM is taken as  $2.5 \mu\text{m}^2$  (59). These parameters result in a room-temperature value of  $\tau_g$  approximately equal to  $20 \mu\text{s}$ , which ensures the DRAM storage cell will not be upset due to the space-charge leakage current. The critical current is modeled to

scale with the DRAM technology generation (e.g., with decreasing  $A_{\text{DRAM cell}}$  due to decreasing CD).

In view of the assumptions made in developing the above models for  $\tau_r$  and  $\tau_g$ , it is not surprising that these parameters do not relate with each other as previously indicated (47,60). Comprehending the periphery, area and volume generation/recombination processes will become more important with the continued miniaturization of silicon device components (61).

#### Gate Oxide Integrity

Gate oxide integrity (GOI) is modeled by the modified Poisson probability distribution of Eq. 5 with the yield  $Y_{\text{Do}} = 99\%$ ,  $R_o = 1$ ,  $\delta = 1$  and  $\beta = 1$  and 10 for the DRAM and MPU, respectively (see Table 9). The GOI is measured at  $10 \text{ MV/cm}$  for  $100 \text{ s}$  under accumulation and  $D_o$  is determined using the charge-to-breakdown,  $Q_{\text{bd}}$ , criteria. The GOI is indicative of potential IC performance, although significant reassessment of the relevance of this methodology is required for sub-4 nm dielectrics (62,63), especially  $< 2 \text{ nm}$ , where direct tunneling current predominates and surface metals may be more detrimental than COPs (64). While other IC electrical parameters such as leakage current, etc. are also important, these parameters were not explicitly addressed in the Starting Materials specifications as they are generally IC design and process dependent.

Table 9  
DRAM and MPU Defect Density With Technology Generation

Year of First Product Shipment Technology Generation	1997 250 nm	1999 180 nm	2001 150 nm	2003 130 nm	2006 100 nm	2009 70 nm	2012 50 nm
$D_{\text{O, DRAM}} (\text{cm}^{-2})$	$\leq 0.06$	$\leq 0.029$	$\leq 0.026$	$\leq 0.014$	$< 0.006$	$< 0.003$	$\leq 0.001$
$D_{\text{O, MPU}} (\text{cm}^{-2})$	$\leq 0.15$	$\leq 0.15$	$\leq 0.11$	$\leq 0.08$	$\leq 0.05$	$\leq 0.04$	$\leq 0.03$

### Oxidation Stacking Faults

Oxidation stacking faults (OSF) are empirically modeled by:

$$OSF = K_5 \times (CD)^{1.42} \text{ (cm}^{-2}\text{)} \quad (17)$$

with  $K_5 = 2.75 \times 10^{-3}$  and CD in nm (15) (see Table 10). The OSF density depends on a number of material and IC

process conditions (7,65,66); the recommended test is steam oxidation at 1100 C for 1 hr and preferential etch after stripping the oxide. Oxidation stacking faults generated during IC fabrication result in competitive and deleterious sinks for metallics compared to bulk  $\text{SiO}_2$  precipitates, due to their proximity to the active device regions. Control of OSF is more difficult in n-type material.

Table 10  
Oxidation Stacking Faults With Technology Generation

Year of First Product Shipment Technology Generation	1997 250 nm	1999 180 nm	2001 150 nm	2003 130 nm	2006 100 nm	2009 70 nm	2012 50 nm
Oxidation Stacking Faults (OSF) (cm <sup>-2</sup> )	≤ 7	≤ 4	≤ 3.5	≤ 3	≤ 2	≤ 1	≤ 1

### Epitaxial Layer Properties

The epitaxial layer thickness represents the range of the center point value with the tolerance expressed as the min-max % range about the selected center point value (see Table 11). The epitaxial layer thickness is empirically modeled from the epitaxial flat-zone required by IC designers by:

$$\text{Epi Layer Thickness} = K_6 \times (\text{Epi Flat-Zone}) \quad (18)$$

with  $K_6 = 1.25$ . The epitaxial growth induced structural defects such as mounds and stacking faults are modeled by the modified Poisson probability distribution of Eq. 3 with the yield  $Y_{\text{EPI}} = 99\%$ ,  $REPI = 1$  and  $\alpha = 1$  (see Table 11). The representation of  $\alpha$  by unity assumes that every defect within the MPU's chip area (which scales with technology generation) is detrimental. Further clarification is expected from ongoing studies of epitaxial defects and defect-specific studies of their impact on GOI and/or junction leakage tests.

Table 11  
Epitaxial Layer Thickness and Defect Density With Technology Generation

Year of First Product Shipment Technology Generation	1997 250 nm	1999 180 nm	2001 150 nm	2003 130 nm	2006 100 nm	2009 70 nm	2012 50 nm
Layer Thickness (μm) (± % Tolerance)	2 - 5 (± 5%)	2 - 4 (± 4%)	2 - 4 (± 4%)	2 - 4 (± 4%)	1 - 3 (± 3%)	1 - 3 (± 3%)	1 - 3 (± 3%)
Layer Structural Defects (cm <sup>-2</sup> )	≤ 0.0033	≤ 0.0029	≤ 0.0026	≤ 0.0023	≤ 0.0019	≤ 0.0016	≤ 0.0013

The improved GOI in epitaxial material is due to the improved structural perfection of epitaxial material as compared to residual polishing micro-damage and grown-in micro-defects in polished wafers. The utilization of polished wafers as well as p/p<sup>-</sup> material with hydrogen or argon annealed substrates for advanced ICs is also receiving attention (67). The benefit of both epitaxial surface quality and reduced system capacitance (due to a larger space-charge region width as a result of the lightly doped substrate) may offset the lack of enhanced solubility gettering of iron in p<sup>-</sup>, compared with conventional p<sup>+</sup> epitaxial, substrates. The oxygen content, however, may have to be re-assessed since oxygen

precipitates slower in p<sup>-</sup>, compared to p<sup>+</sup>, material (34,68), at least for conventionally prepared materials. Back-surface polysilicon gettering may become more fully utilized, in conjunction with the general reduction of the oxygen content, in both epitaxial substrates and polished wafers (69). Selection of the gettering system, however, is very dependent on the IC thermal process sequence. The role of MeV implantation and associated annealing procedures in polished wafers as a replacement for epitaxial structures continues to receive attention, although the control of COPs and related defects is aggravated in polished wafers. The use of MeV implant/thermal anneal procedures, in conjunction with

epitaxial wafers, has also been proposed to achieve enhanced device architectures.

### Silicon-On-Insulator

The silicon layer thickness represents the range of the center point value with the tolerance expressed as the min-max % range about the selected center point value (see Table 12). The buried oxide (BOX) thickness represents the range of the center point value with the tolerance expressed as the min-max % range about the selected center point value. A fully depleted silicon layer is anticipated for  $CD < 100$  nm, dependent on the IC application and is reflected in the silicon thickness (in conjunction with the BOX thickness) required to withstand the device breakdown voltage. The interface charge at the SOI/BOX interface is specified to be  $< 1 \times 10^{11}/\text{cm}^2$ .

The three types of SOI defects examined are BOX defects, inclusions and threading dislocations (70); these

defects have been calculated independently at the 99% level for the case of an MPU. The BOX defect density,  $D_{\text{BOX}}$ , is modeled by the modified Poisson probability distribution Eq. 5 with the yield  $Y_{\text{BOX}} = 99\%$ , BOX kill ratio  $R_{\text{BOX}} = 0.2$ ,  $\beta = 10$  and  $\delta = 6$ . The six CD units for  $\delta$  are represented as the gate, the sidewall spacers, and the salicided source and drain. The inclusion density,  $D_{\text{INC}}$ , is modeled with the yield  $Y_{\text{INC}} = 99\%$ , inclusion defect kill ratio  $R_{\text{INC}} = 1$ ,  $\beta = 10$  and  $\delta = 1$  (gate). The threading dislocation density,  $D_{\text{TD}}$ , is modeled with the yield  $Y_{\text{TD}} = 99\%$ , threading dislocation kill ratio  $R_{\text{TD}} = 1 \times 10^{-6}$ ,  $\beta = 10$  and  $\delta = 2$ . The 2 CD units arise from the gate and the sidewall spacers, where the dislocations could impact the gate oxide or p-n junctions, respectively. The selection of the kill ratios is expected to require re-assessment. It also appears that a two-way partitioning of the BOX defects and inclusions (e.g., to be expanded to reflect pits/COPs as well as inclusions) may be appropriate while threading dislocations may not be particularly harmful (71).

Table 12  
SOI Layer Thickness and Defects With Technology Generation

Year of First Product Shipment Technology Generation	1997 250 nm	1999 180 nm	2001 150 nm	2003 130 nm	2006 100 nm	2009 70 nm	2012 50 nm
Silicon Layer Thickness (Tolerance $\pm 5\%$ ) (nm)	50 - 200	50 - 200	50 - 200	50 - 200	50 - 100	30 - 100	20 - 100
Buried Oxide Thickness (Tolerance $\pm 5\%$ ) (nm)	$\leq 400$	$\leq 200$	$\leq 200$	$\leq 200$	$\leq 100$	$\leq 70$	$\leq 50$
$D_{\text{BOX}}$ , MPU (Box Defects) ( $\text{cm}^{-2}$ )	$\leq 0.12$	$\leq 0.12$	$\leq 0.09$	$\leq 0.06$	$\leq 0.04$	$\leq 0.03$	$\leq 0.02$
$D_{\text{INC}}$ , MPU (Inclusions) ( $\text{cm}^{-2}$ )	$\leq 0.15$	$\leq 0.15$	$\leq 0.11$	$\leq 0.08$	$\leq 0.05$	$\leq 0.04$	$\leq 0.03$
$D_{\text{TD}}$ , MPU (Threading Dislocations) ( $\text{cm}^{-2}$ )	$\leq 7.2 \times 10^4$	$\leq 7.4 \times 10^4$	$\leq 5.6 \times 10^4$	$\leq 3.9 \times 10^4$	$\leq 2.6 \times 10^4$	$\leq 2.0 \times 10^4$	$\leq 1.4 \times 10^4$

Evaluation of the various SOI wafer fabrication techniques by material characterization and identification of the relationships between defects and SOI properties such as gettering and the effective SOI recombination lifetime (see Table 8) on subsequent device properties is essential (71). The small SOI supplier base impacts the cost structure although different SOI approaches may be necessary to service different IC applications. Some bulk IC designs can be directly transferred to SOI. Process and mask redesign may further improve performance and chip size. However, SOI applications may be limited until conventional silicon materials reach a technological or economic wall, perhaps at 130 nm and beyond. Nevertheless, SOI obviates the concern about latch-up while offering the potential for improved device performance, soft-error immunity, low-power applications, fewer process steps and, presumably,

smaller chip size with the associated opportunity of utilizing the previous generation's factory equipment to achieve the required number of chips per wafer.

### SUMMARY

For technology generations down to 100 nm, the CoO of silicon material quality, both polished and epitaxial wafers, is of paramount importance. This includes distinguishing particles, microroughness and silicon micro-defects for the front-surface (and, where the requisite instrumentation is available, for the back-surface) with improved understanding and control of both grown-in micro-defects and the wafer-carrier interaction, and their subsequent impact on relevant device characteristics. The critical challenge for technology generations below 100 nm is the CoO for the production of 450 mm, 675 mm and SOI starting materials. The

methodology for fabricating silicon for the 64 Gbit era (450 mm and 675 mm wafers) as compared to the effective introduction of SOI and compatibility with IC processing needs to be established. The engineering issues associated with these larger diameters, however, appear to be enormous and a paradigm shift in approaching the fabrication of cost-effective silicon materials, including the cost-effective introduction of SOI, is required. The manufacturing cost for the 450 mm and larger diameter wafers, for example, is projected to become both an increasing percentage and increase the total device manufacturing cost (72). The fabrication of silicon materials on an appropriate substrate or re-engineering the IC package could help mitigate the escalating costs associated with grinding off approximately 50% of the wafer volume, as is currently done with conventional silicon materials and IC packages.

In addition to the effective partitioning of relevant material parameters, it will be essential to incorporate the defect size distribution and kill ratio in the Poisson probability distribution as well as identify improved kill factors for the various defects. The de-convolution of particles, COPs and microroughness for the front-surface remains critical as the CD is approaching the COPs grown-in dimensions. Back-surface particle detection may be limited to  $\geq 200$  nm, even for smaller CD, as a result of the back-surface finish. The improvement in back-surface finish compared to current standards, however, will more readily exhibit microscopic contamination and handling scratch damage from robotic handling systems. Standards for robotic handlers, therefore, may be necessary to ensure conformance of the surface to the implicit cleanliness requirements. The characterization of the surface microroughness is essential inasmuch as the excursion of microroughness may be comparable to the gate dielectric thickness, which may be only several unit cells thick, at least for the silicon dioxide, oxynitride and silicon nitride dielectric systems. Finally, determination of material parameters over the whole wafer surface (taking cognizance of the edge exclusion) is a most critical metrology issue.

## FUTURE OPPORTUNITIES

To reduce the CoO of wafers, the silicon supplier parameter distributions should be utilized as materials acceptance criteria at IC companies. This method would alleviate the challenge of separating measurement variability from the true parameter variability that is becoming more difficult as the values for many parameters are approaching detection or resolution limits. Use of parameter distributions established by wafer suppliers for their processes to demonstrate that an ensemble of wafers will be satisfactory for the intended purpose will require improvements in both process

capabilities and a significant paradigm shift in IC materials acceptance practices. Currently available models, however, cannot sufficiently establish the real requirements for parameter uniformity or the effects of parameter variability on IC properties. The requirements presented in the 1997 edition of the Starting Materials Roadmap do not adequately address either of these issues and development of such models will be essential to enhance the utility of future Roadmaps.

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